REMARKS

In view of the above amendments and the following remarks, reconsideration is hereby requested.

Various editorial amendments have been made to the specification. No new matter has been added.

Claims 3-9, and 11-36 were indicated as allowed, and claims 2 and 10 were indicated to be allowable if rewritten in independent form to include the limitations of base claim 1.

The claims have been reviewed and revised in order to improve their U.S. form. It is submitted that claims 2-36 as amended remain allowable for same the reasons for the indication of allowable subject matter by the Examiner in the last Office Action.

However, it is requested that the Examiner reconsider claim 1, which was rejected under 35 U.S.C. § 102(e) as being anticipated by Hiratsuka (US 7012862), in light of the clarifying amendments to claim 1 herein and the following remarks.

As illustrated in Figs. 2 and 3 of the present application, according to the present invention, the phase comparison output for each comparison is output at only one clock, i.e., only during one clock period of the sampling clock. As shown in figures 3(a) and 3(b), the output amplitude for each pulse of the phase difference detection circuit is larger at the inner track where the number of sampling within a predetermined phase interval is relatively large than at the outer track where the number of sampling within the same phase interval is relatively small. However, since the phase comparison result is output at only one clock, the time required for outputting the phase comparison result is shorter at the inner track than at the outer track. Therefore, when a tracking error signal is generated by subjecting the phase comparison result to band restriction by a low pass filter, the amplitude of the tracking error signal at the inner track becomes equal to that at the outer track. In this way, dependence of the tracking error signal on the linear velocity during CAV playback can be resolved.

Accordingly, claim 1 recites a phase difference detection circuit that outputs a result of phase comparison obtained between the respective zerocross points as a pulse signal having a pulse width corresponding to one period of a sampling clock, and a low-pass filter that performs band restriction to a signal outputted from the phase difference detection circuit to obtain a tracking error signal.

Hiratsuka (US 7012862) does not disclose such features. Rather, Hiratsuka (US 7012862) discloses that after the phase difference circuit 19 detects the phase difference between the respective zerocross points in the two waveforms, it holds the output level of the phase difference signal that is obtained at the previous zerocross point up to the next zerocross point, as shown in Figure 13. Therefore, claim 1 is not anticipated by Hiratsuka (US 7012862).

In view of the above amendments and remarks, it is submitted that claims 1-36 are allowable over the prior art of record, and that the present application is in condition for allowance.

The Examiner is invited to contact the undersigned by telephone to resolve any remaining issues.

Respectfully submitted,

Takashige HIRATSUKA et al.

By: _____
Jeffrey R. Filipek
Registration No. 41,471
Attorney for Applicants

JRF/fs
Washington, D.C. 20006-1021
Telephone (202) 721-8200
Facsimile (202) 721-8250
March 7, 2007